The Impact of Maximum Vector Length on Cache Management Techniques in RISC-V Vector Extension

Shunya Nomura
Graduate School of Information Sciences,
Tohoku University
Sendai, Miyagi, Japan
nomura.shunya.r5@dc.tohoku.ac.jp

Jiaheng Liu
RIKEN Center for Computational Science
Kobe, Hyogo, Japan
jiaheng.liu@riken.jp

Keichi Takahashi
D3 Center, The University of Osaka
Toyonaka, Osaka, Japan
Cyberscience Center, Tohoku University
Sendai, Miyagi, Japan
keichi@tohoku.ac.jp

Hiroyuki Takizawa
Cyberscience Center, Tohoku University
Sendai, Miyagi, Japan
takizawa@tohoku.ac.jp

1 Introduction

In recent years, computers have faced increasing demands for energy efficiency. Single Instruction Multiple Data (SIMD) execution exploits data-level parallelism (DLP) to enable efficient processing. RISC-V [6], an open-source instruction set architecture, provides the RISC-V Vector Extension (RVV) as its SIMD-style instruction set. In RVV, the instruction's vector width is decoupled from the hardware datapath width, allowing the same binary to execute on processors with varying Maximum Vector Length (MVLs).

Since RVV leverages DLP, a single vector instruction can operate on many data elements in parallel. Consequently, effective cache management is critical to accelerate data movement and keep supplying data to functional units. Indeed, Gómez et al. [3] employed cache bypassing for low-locality data as part of optimizing HPCG on a vector processor. While such cache-targeted optimizations exist, to our knowledge there has been no report on systematic evaluation of cache management techniques across different MVLs. Changes in MVL can plausibly alter cache access behavior; for example, alignment effects are frequently discussed in vector computing and are particularly salient for shorter vector lengths, where the performance impact of unaligned accesses is more pronounced.

In this paper, we focus on two cache management techniques: cache replacement policies and non-temporal hints. We hypothesize that, even for the same program under RVV, processors with different MVLs exhibit distinct memory-access patterns, which in turn can change the choice of the most effective cache management techniques. Our goal is to clarify how the MVL of a processor influences the efficacy of cache management under RVV.

2 Evaluated Cache Management Techniques

This paper focuses on cache management techniques, specifically replacement policies and non-temporal hint instructions.

2.1 Replacement Policies

A replacement policy is an algorithm that determines which cache line to evict when a new cache line is inserted into the cache. In this paper, we compare the following three replacement policies.

- Least Recently Used (LRU)
- Static Re-Reference Interval Predictor (SRRIP) [1]
- Signature-based Hit Predictor (SHiP) [2]

LRU, the most fundamental replacement policy, leverages temporal locality by expecting that recently accessed lines will be re-referenced in the near future. SRRIP employs a value called the Re-Reference Prediction Value (RRPV) to learn access patterns and selects the victim line based on its RRPV. The SHiP policy uses signatures to capture access patterns, incorporating the learned results into the RRPV assignment when inserting cache lines, similar to SRRIP.

2.2 Non-Temporal Hints

A non-temporal hint explicitly indicates low memory access locality to the cache, thereby preventing cache pollution. In this paper, we evaluate three methods for utilizing non-temporal hints.

- Cache Bypass
- Hint-assisted RRIP (HRRIP)
- Hint-assisted LRU (HLRU)

In Cache Bypass, when a memory access is marked with a low-locality hint, a cache miss does not trigger the allocation of a new cache line. In HRRIP and HLRU, when such a hint is provided, the new cache line is inserted with the lowest replacement priority, making it more likely to be evicted.

3 Evaluation

In this paper, we employ a gem5-based implementation of a RISC-V vector processor model [4, 5]. The benchmarks are selected from the RISC-V Vectorized Benchmark Suite (RiVEC) [4], specifically jacobi-2d and spmv. For both benchmarks, aligned versions of the matrices or arrays are also prepared to examine the impact of alignment. Using these benchmarks, we compare six cache management techniques.

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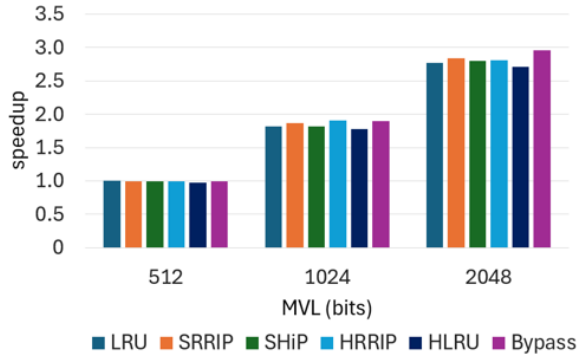
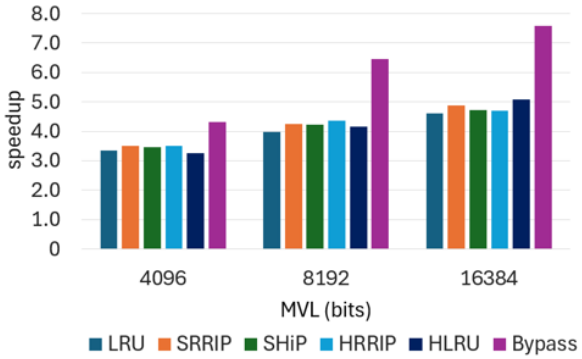
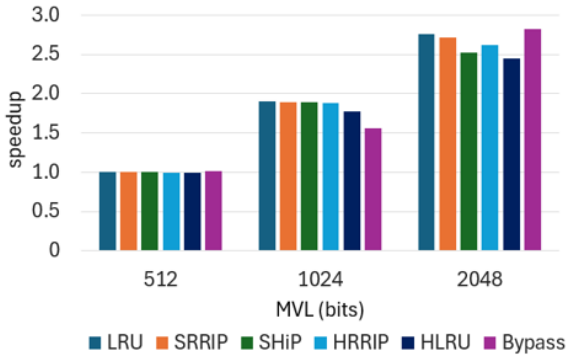


(a) For MVLs ranging from 512 bits to 2048 bits.

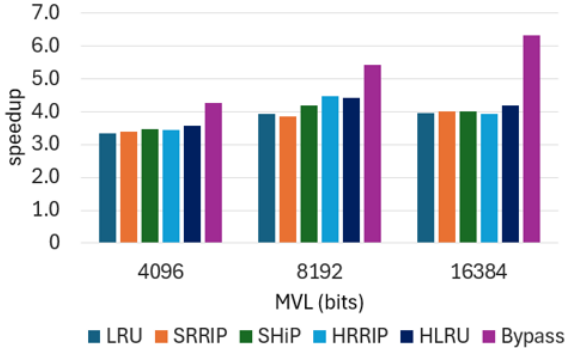


(b) For MVLs ranging from 4096 bits to 16384 bits.

Figure 1: Speedup of jacobi-2d for each MVL and cache management technique (normalized to the case of LRU with MVL = 512 bits).



(a) For MVLs ranging from 512 bits to 2048 bits.



(b) For MVLs ranging from 4096 bits to 16384 bits.

Figure 2: Speedup of aligned jacobi-2d for each MVL and cache management technique (normalized to the case of LRU with MVL = 512 bits).

Figure 1 shows the jacobi-2d results for different cache management techniques. The optimal technique depends on the MVL, with cache bypass showing the largest performance variation due to MVL-induced changes in access patterns. Since both scalar and vector instructions access the working set, changes in MVL alter the runtime vector length and the frequency of scalar accesses, thereby modifying the access pattern. Figure 2 shows the comparison results when data are aligned to cache-line boundaries. Compared to the unaligned case, the performance trends of the cache management techniques differ, indicating that alignment alters access patterns and influences the effectiveness of cache management.

Figure 3 shows the comparison results for spmv. In contrast to jacobi-2d, the performance trends across cache management techniques are more consistent. However, in the case of cache bypass, performance degradation is observed for short MVLs. This is likely because the impact of unaligned accesses varies with MVLs. Indeed, when arrays are aligned, as shown in Figure 4, the performance drop disappears. These results indicate that, for certain cache management techniques, the performance impact of unaligned accesses depends on MVL, leading to MVL-dependent performance variation.

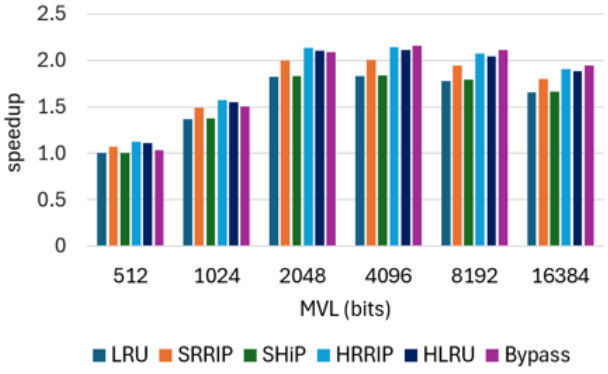


Figure 3: Speedup of spmv for each MVL and cache management technique (normalized to the case of LRU with MVL = 512 bits).

4 Conclusion

The evaluation results in this paper Our results demonstrated that the optimal cache management technique can vary depending on

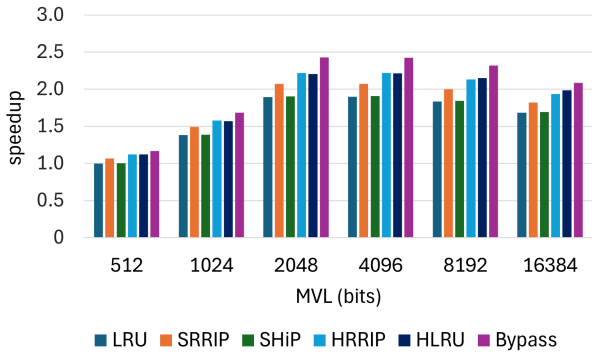


Figure 4: Speedup of aligned spmv for each MVL and cache management technique (normalized to the case of LRU with MVL = 512 bits).

MVL. This variation arises from two key factors: (1) the MVL-dependent change in the ratio between vector and scalar memory instructions, and (2) the MVL-dependent change in the impact of misalignment. These findings highlight the necessity of considering MVL, alongside application characteristics, when selecting appropriate cache management techniques. A technique that is effective on a system with a specific MVL is not necessarily effective on systems with other MVLs.

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